

U.S. Patent Application Serial No. 10/813,085
Amendment filed April 18, 2006
Reply to OA dated October 18, 2005

REMARKS

Claims 1-15 are pending, with claims 13-15 withdrawn from consideration. Claim 8 is amended herein. Upon entry of this amendment, claims 1-15 will be pending, with claims 13-15 withdrawn from consideration. Entry of this amendment and reconsideration of the rejections are respectfully requested.

No new matter has been introduced by this Amendment. Support for the amendments to the claims is discussed below.

The title of the invention is not descriptive. (Office action paragraph no. 2)

Reconsideration of the objection is respectfully requested. The Examiner does not explain why he considers the title not to be descriptive. The Examiner may be referring to the fact that the method claims were not elected and are currently withdrawn from consideration. However, since claims 13-15 are still pending, Applicant has not amended the title.

Claim 8 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. (Office action paragraph no. 3)

The Examiner indicates that the phrase “at least one portion having the compositional ratio x which exceeds the above-described range” is unclear because claim 4 does not recite a range for x.

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The rejection of claim 8 is overcome by the amendment to claim 8, which has been amended herein to depend from claim 7. In addition, "include" in claim 8 has been amended to --includes--, for grammatical reasons.

Claims 4 and 8 are rejected under 35 U.S.C. §102(e) as being anticipated by Yoshida et al. (US 6,897,495). (Office action paragraph no. 4)

The rejection of claims 4 and 8 is traversed, and reconsideration of the rejection is respectfully requested.

In the present invention, claim 4 recites: "a stack formed on a substrate, said stack comprising" first, second and third semiconductor layers, with "all of the layers being sequentially grown on said substrate." In Fig. 9 of the present application, for example, these are sequential layers 2, 3 and 4. That is, according to claim 4 of the present invention, an n-GaN is formed under the gate electrode.

In contrast, in Fig. 1B, Yoshida discloses n⁺-type GaN contact region 24b (the third nitride semiconductor layer) being alongside of electron transit layer 14 (the first nitride semiconductor layer) and Al_{0.2}Ga_{0.8}N electron supply layer 16 (the second nitride semiconductor layer), not on top of these layers. The n-GaN is formed on the portion except under the gate electrode, and AlGa_{0.8}N is selectively buried only under the gate electrode. Accordingly, **the structure of the present invention is different from that of Yoshida.**

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Furthermore, Applicant respectfully notes that the Examiner is incorrect in stating that “no compositional ratio of Al of any layer is provided” In column 6, lines 1-9, of Yoshida, an n-GaN contact region 24b has $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ electron supply layer 16 of thickness 30 nm. The value of x is therefore 0.2 in this case.

Moreover, claim 4 requires that the relation $-80x + 29 < d < x - 180x + 52$ be satisfied. In case of the value of $x = 0.2$, this relation would require the thickness d to be: $13 < d < 16$. The value of $d = 30$ in Yoshida **does not satisfy the relation recited in claim 4**. Therefore, this disclosure in Yoshida clearly **does not anticipate claim 4**, and there appears to be no suggestion in the reference for the recited relation in claim 4.

Since Yoshida neither discloses nor suggests the structure or the compositional relation recited in claim 4, claims 4 and 8 are not anticipated by, and further, are not obvious over, Yoshida et al. '495.

Claims 5-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshida et al. (US 6,897,495). (Office action paragraph no. 5)

The Examiner states that Yoshida et al. does not teach the thickness of the third nitride semiconductor layer (i.e., Yoshida's n^+ -type GaN contact region 24b) and the sheet resistance of the stack, but that these would have been obvious “result effective variables.”

The rejection of claims 5-7 is respectfully traversed. As noted above, base claim 4 is not anticipated by, nor obvious over, Yoshida. As noted above, the three layers cited by the Examiner

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do not form a stack, and therefore are inconsistent with the structure recited in claim 4. Moreover, as noted, Yoshida's $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ electron supply layer 16 is inconsistent in thickness with the second nitride semiconductor layer of claim 4.

In addition, it is clear in Yoshida's Fig. 1B that the thickness of n^+ -type GaN contact region 24b is slightly greater than the **combined** thickness of layers 14 and 16, since layer 24b is alongside layers 14 and 16. Clearly, layer 24b in Yoshida cannot be less than 10 nm, since layer 16 is 30 nm thick (column 6, line 7).

Further, the Examiner has not indicated what is the parameter (i.e., the “result”) that would be optimized by modifying the “result-effective variables” in Yoshida. The stated motivation of “discovering an optimum” in Yoshida is therefore improper. In addition, it is clear that no modification of the thicknesses of Yoshida's layers could produce the structure recited in the present claims.

Claims 5-7 are therefore not obvious over Yoshida et al. '495.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the Applicant's undersigned agent at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

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In the event that this paper is not timely filed, the applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosure: Petition for Extension of Time

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